

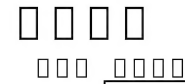
**FL100**

[illegible]

A diagram showing a sequence of 100 boxes arranged in 10 rows of 10. The first 99 boxes are empty, and the 100th box contains a minus sign (-).

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Figure 1 illustrates the architecture of the proposed CPEVS-1P. The system consists of eight processing blocks arranged in a sequence. The first four blocks are labeled DD (09), AT (03), DT (01), and DR (00). The next four blocks are labeled DT (00), DR (01), AR (03), and DD (08). Each block contains a shaded vertical rectangle, which represents a CPEVS-1P component. Arrows indicate the data flow between these blocks and to/from a central point. A legend indicates that the shaded rectangles represent CPEVS-1P components.

[illegible][illegible][illegible]